30nm Physical Gate Length CMOS Transistors with 1.0 ps n-MOS and 1.7 ps p-MOS Gate Delays

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I. Abstract

Planar CMOS transistors have been fabricated to evaluate the 70nm technology node using conventional transistor design methodologies. Conventional CMOS transistors with 30nm physical gate length were fabricated using aggressively scaled junctions, polysilicon gate electrode, gate oxide and Ni silicide. These devices have inversion Cox exceeding 1.9μF/cm2, n-MOS gate delay (CV/I) of 0.94 ps and p-MOS gate delay of 1.7 ps at V_{cc}=0.85V. These are the smallest CV/I values ever reported for Si CMOS devices. The transistors also show good short channel control and subthreshold swings. The n-MOS and p-MOS have drive currents equal to 514μA/μm and 285μA/μm respectively with I_{off} at or below 100nA/μm at Vcc=0.85V. The saturation gm is equal to 1200mS/mm for n-MOS and 640mS/mm for p-MOS. These are among the highest gm values ever reported. The junction edge leakage is reasonably low with less than 1nA/um at 1.0V and 100C for both n-MOS and p-MOS. These encouraging results suggest that the 70nm technology node is achievable using conventional planar transistor design and process flow.

II. Introduction

The difficulties of the continued scaling of CMOS transistors and industry's ability to continue the Moore's Law scaling trend have received much attention recently [1-4]. The ability to produce transistors with reasonable short-channel effect and device performance at the 70nm technology node (physical gate length of about 30nm) has been highlighted as an area of significant concern. Recent studies suggest that transistors with gate lengths at or below 30nm with controllable short channel effects are difficult to achieve [2], and that non-planar device structures may be needed [5-7]. Thus it is of great importance to fabricate conventional CMOS transistors with physical gate length of about 30nm and characterize their functionality and performance for logic applications. In this paper, we report the n-and p-MOS performance results for CMOS transistors with inversion C_{ox} exceeding 1.9μF/cm^2 and physical gate lengths down to 30nm. The devices were fabricated using conventional planar CMOS process flow.

III. Transistor Features

a) Lithography: In order to achieve the desired gate length dimensions, a standard two-mask phase shift mask approach was used. This approach enabled the fabrication of 30nm polysilicon lines using 248nm lithography with over-exposure. Figure 1 shows a top-down SEM micrograph of a transistor with a gate length of 30nm and a gate width of 0.21 μm. The polysilicon line edge roughness is $\pm$ 5 nm. Figure 2 shows the corresponding cross-sectional TEM image of the transistor with physical gate length of 30nm.

b) Gate Stack: Physical gate oxide and polysilicon gate electrode thickness were aggressively scaled to sub-1.0nm and below 100nm respectively in order to achieve high drive currents and controllable short channel effects. Figure 3 shows a TEM cross-section of the sub-1.0nm gate oxide. Figure 4 shows the inversion C-V characteristics of the resulting gate stack measured using a novel transmission line methodology [8]. An inversion capacitance exceeding 1.9 μF/cm^2 was achieved for both p- and n-MOS.

c) Well and SD-Extension Engineering: In order to control short channel effect and achieve sufficiently low external resistance and overlap capacitance, retrograded wells, aggressively scaled S/D and S/D extensions, and thermal anneal temperatures below 1000^{o}C were used. No halo implant was used in the process flow. To minimize poly depletion effect with scaled junctions, the polySi gate thickness was scaled to below 100nm.

d) Silicide Engineering: In order to ensure that the silicide resistances are sufficiently low for polysilicon line width less than 50nm, Ni silicide was used [9].

IV. Results and Discussion

The n-MOS device characteristics with 30nm physical gate length are shown in Figures 5 and 6. Figure 5 shows the I_d-V_g characteristics measured at V_d=0.05V and V_d=0.85V. Figure 6 shows the I_d-V_d characteristics for different applied gate voltages. It can be seen that the device has I_{off} of 100nA/μm at V_{cc}=0.85V, subthreshold swing of 100mV/decade at V_{cc}=0.85V, and a DIBL effect of about 100mV. These results suggest that the device has controllable short channel effect. The drive current for this device is 514 μA/μm at V_{cc}=0.85V.

For the 30nm p-MOS transistor, the characteristics are shown in Figures 7 and 8. The p-MOS device exhibits I_{off} of 83 nA/μm at V_{cc}=0.85V, subthreshold swing of 100mV/decade at V_{cc}=0.85V, and a DIBL effect of about

100mV. This device gives a drive current of 282 μA/μm at V_{cc}=0.85V. These results show the p-MOS device has controllable short channel effect with reasonably good drive current.

The saturation transconductance (gm) curves of the n-MOS and p-MOS transistors are plotted in Figures 9 and 10 respectively. The peak saturation gm is equal to 1200mS/mm for n-MOS and 640mS/mm for p-MOS. These are among the highest gm values ever reported for conventional Si CMOS transistors.

Figure 11 shows the junction edge leakage (I_{JE}) plots of the n-MOS and p-MOS transistors with 30nm physical gate length at 25°C and 100°C. I_{JE} is dominated by the parasitic tunneling reverse leakage in the source and drain of the transistor, and potentially can limit transistor scaling [3,10]. The measurement results show that at 1.0V and 100°C, I_{JE} is reasonably low with less than 1.0nA/um for both n-MOS and p-MOS, which is less than 5% of the transistor I_{off}. The data indicates junction edge leakage will not be a concern for the 70nm technology node.

The CMOS transistors achieve n-MOS gate delay (CV/I) of 0.94 ps as shown in Figure 12, and p-MOS gate delay of 1.7 ps as shown in Figure 13, at V_{cc}=0.85V. These are the smallest CV/I values ever reported for Si CMOS devices [11-17]. These CV/I results, combined with the excellent I_{on}-I_{off} performance and junction edge leakage characteristics, suggest the 70nm technology node can be achieved with i) the use of conventional planar transistor design and process flow, and ii) with the continual push of process technologies such as gate dielectric and lithography.

V. Conclusions

Results are reported on conventional n-MOS and p-MOS devices fabricated using aggressive scaling of the transistor features. The physical gate lengths measure 30 ± 5nm and were achieved using 248 nm phase shift mask lithography. The devices were fabricated with aggressive scaling of gate oxide, junctions, polysilicon gate and Ni silicide. An inversion capacitance exceeding 1.9 $\mu F/cm^2$ was achieved for both p- and n-MOS with the use of sub-1.0nm gate oxide. These devices show excellent I_{on}-I_{off} performance with I_{on}=514μA/μm for n-MOS and 285μA/μm for p-MOS with I_{off} at or below 100nA/μm at Vcc=0.85V. The CV/I gate delay is 0.94ps for n-MOS and 1.7 ps for p-MOS. These CV/I values are the lowest ever reported for Si CMOS devices. The saturation gm values are 1200 mS/mm and 640 mS/mm for n-MOS and p-MOS respectively. The junction edge leakage is less than 1nA/um for both n- and p-MOS at 1.0V and 100C. These encouraging results suggest that the 70nm technology node is achievable with the use of conventional planar CMOS transistor design and process flow, and with the continual push of process technologies such as lithography and gate dielectric.

VI. Acknowledgements

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VII. References

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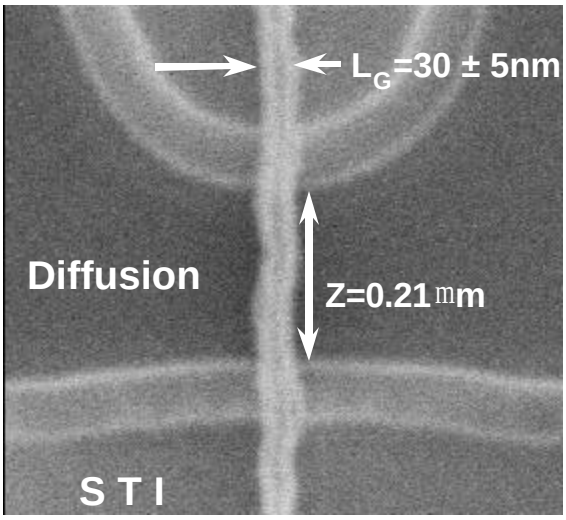

Fig. 1 Top-down SEM of the 30nm poly-silicon line fabricated using 248 nm phase shift mask lithography. The line edge roughness is ± 5nm.

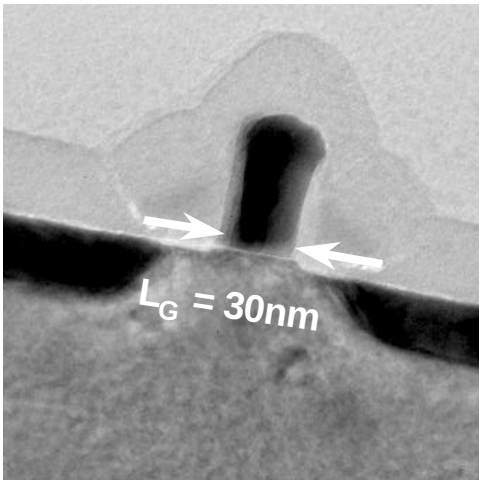

Fig. 2 Cross-sectional TEM of a transistor with 30nm physical gate length.

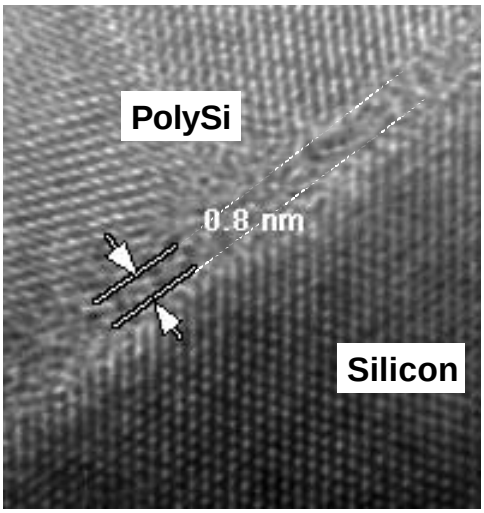

Fig. 3 Cross-sectional TEM of the gate stack.

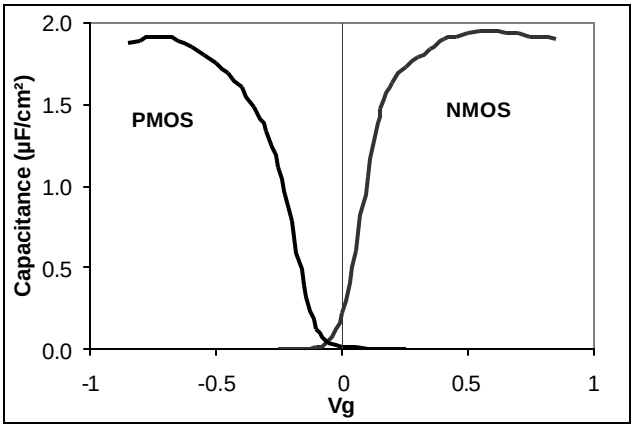

Fig. 4. Inversion C-V of the p-MOS (left) and n-MOS (right) gate oxide.

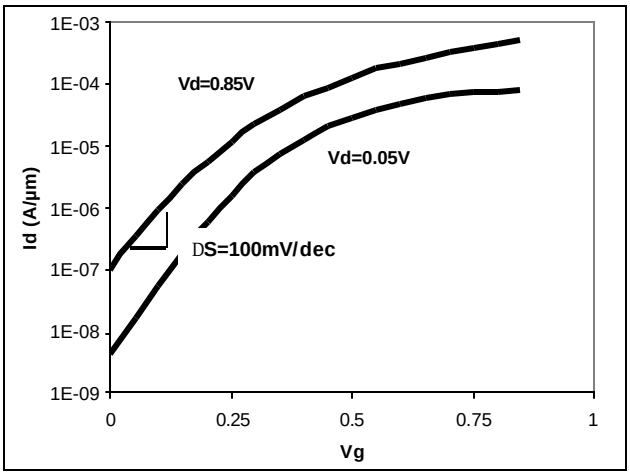

Fig. 5 MOSFET sub-threshold I_d-V_g curves for the 30nm n-MOS device.

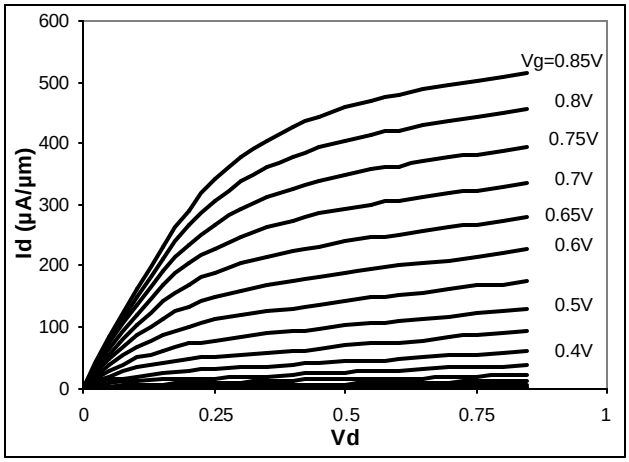

Fig. 6 MOSFET I_d-V_d curves for the 30nm n-MOS device.

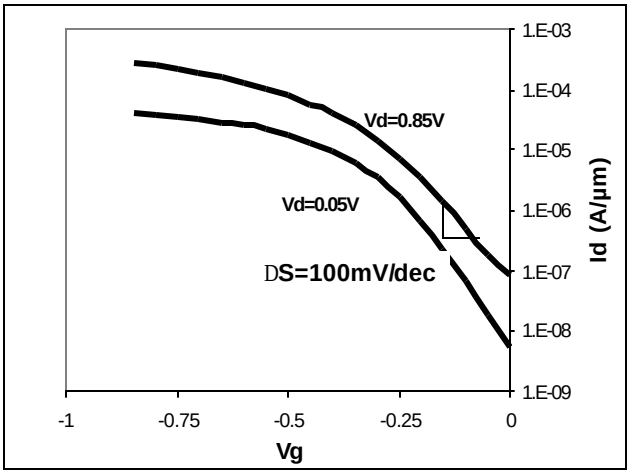

Fig. 7 MOSFET sub-threshold I_d-V_g curves for the 30nm p-MOS device.

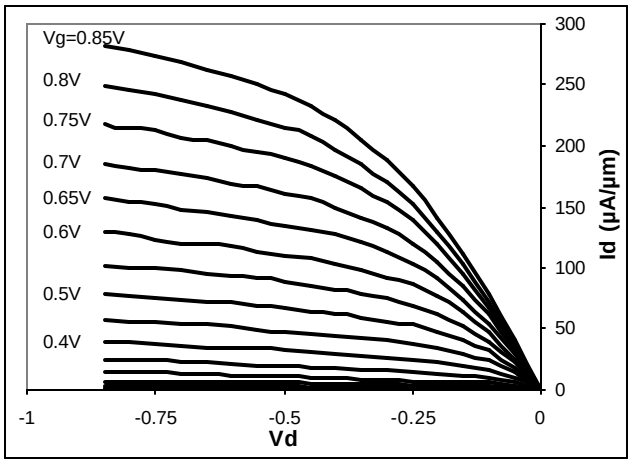

Fig. 8 MOSFET I_d-V_d curves for the 30nm p-MOS device.

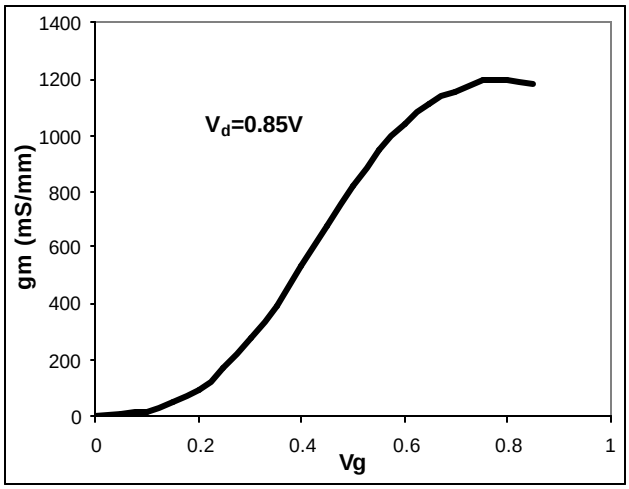

Fig. 9 Saturation transconductance (gm) curve of the 30nm n-MOS transistor with peak gm equal to 1200mS/mm.

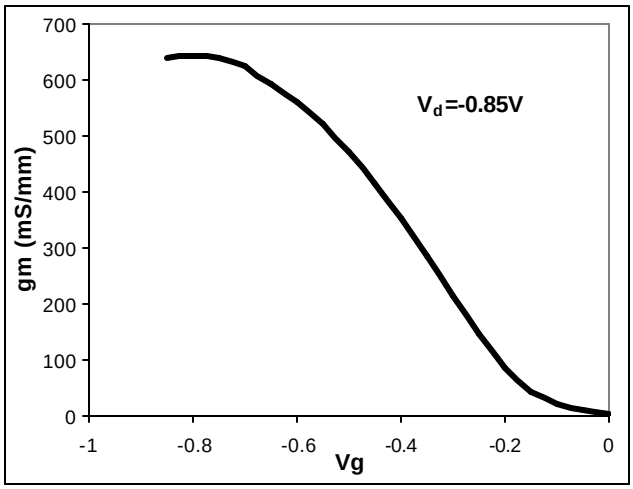

Fig. 10 Saturation transconductance (gm) curve of the 30nm p-MOS transistor with peak gm equal to 640mS/mm.

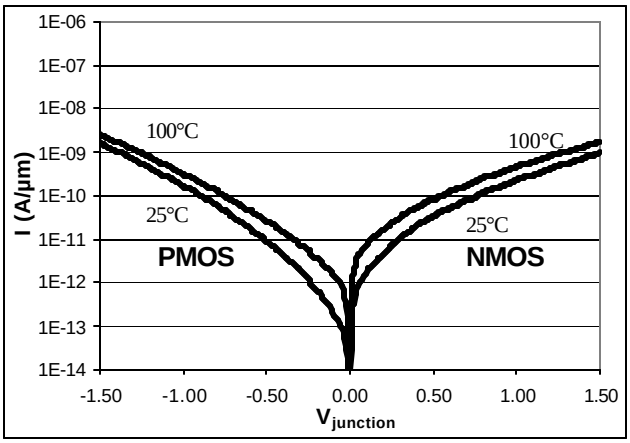

Fig. 11 Junction edge leakage of the 30nm p-MOS (left) and n-MOS (right) at 25°C and 100°C.

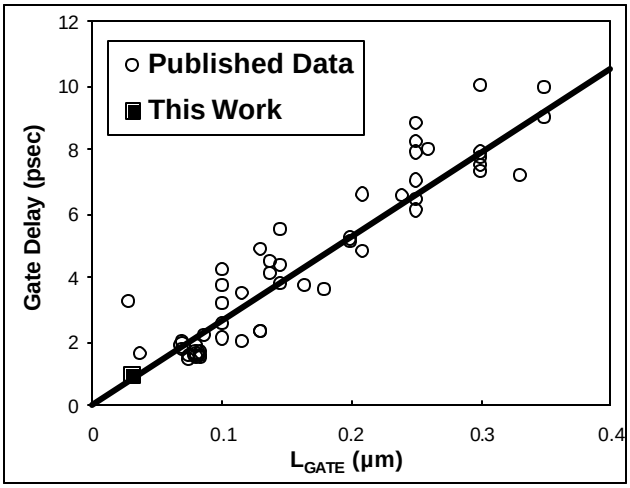

Fig. 12 n-MOS transistor gate delay (CV/I) versus physical gate length trend.

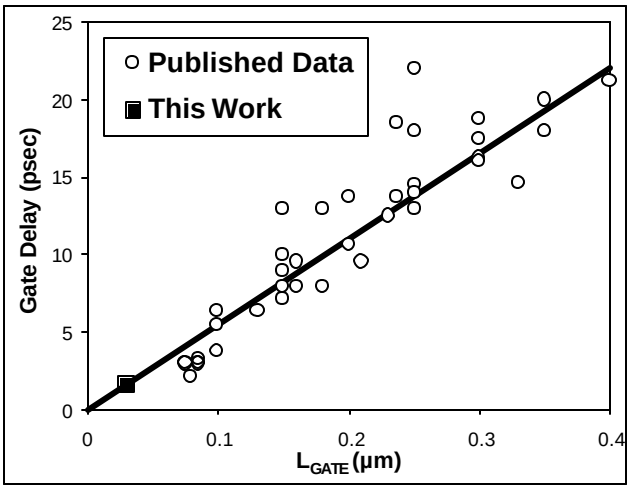

Fig. 13 p-MOS transistor gate delay (CV/I) versus physical gate length trend.